

**FIG. 1.**  
(PRIOR ART)

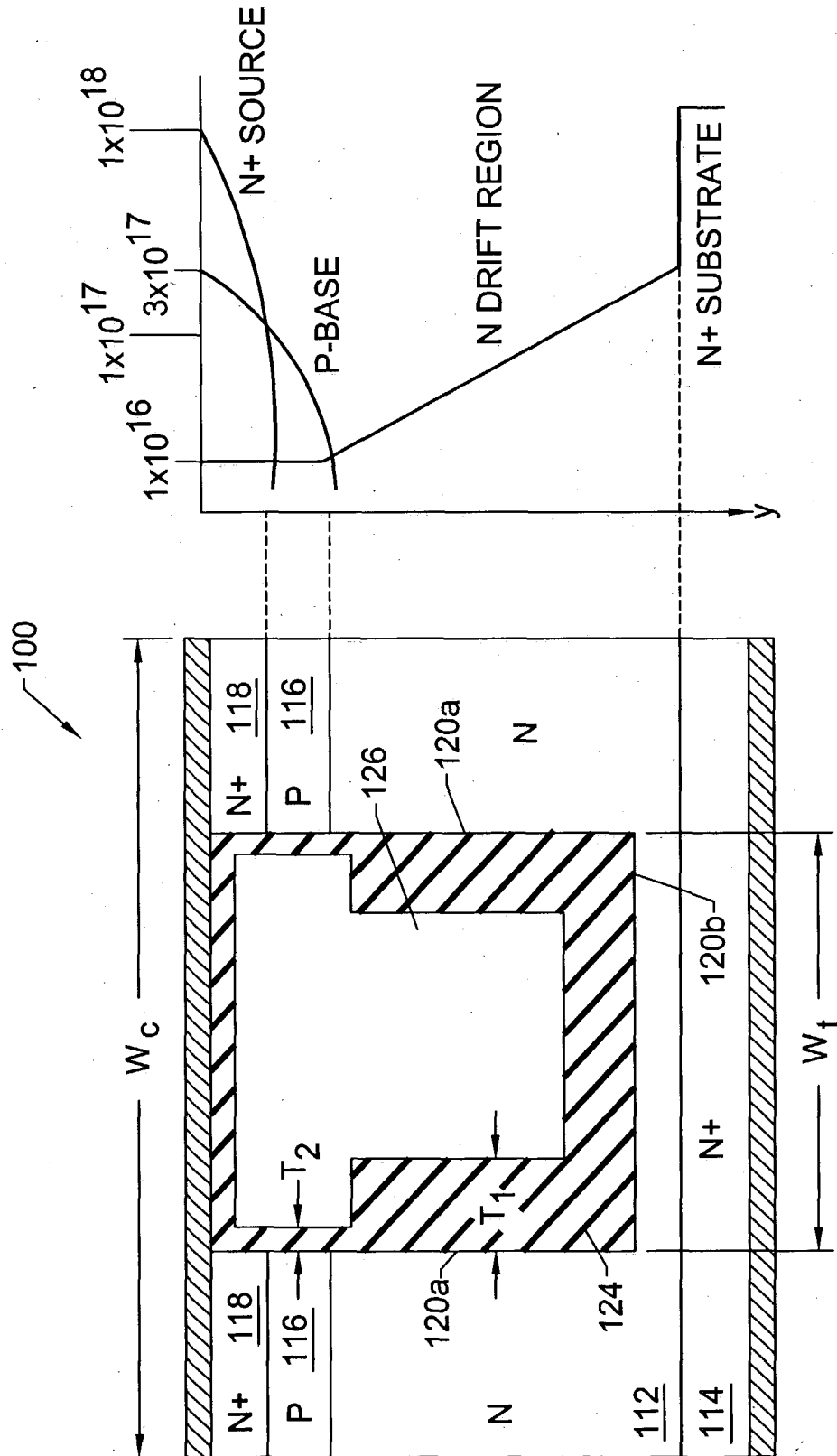


FIG. 2.  
(PRIOR ART)

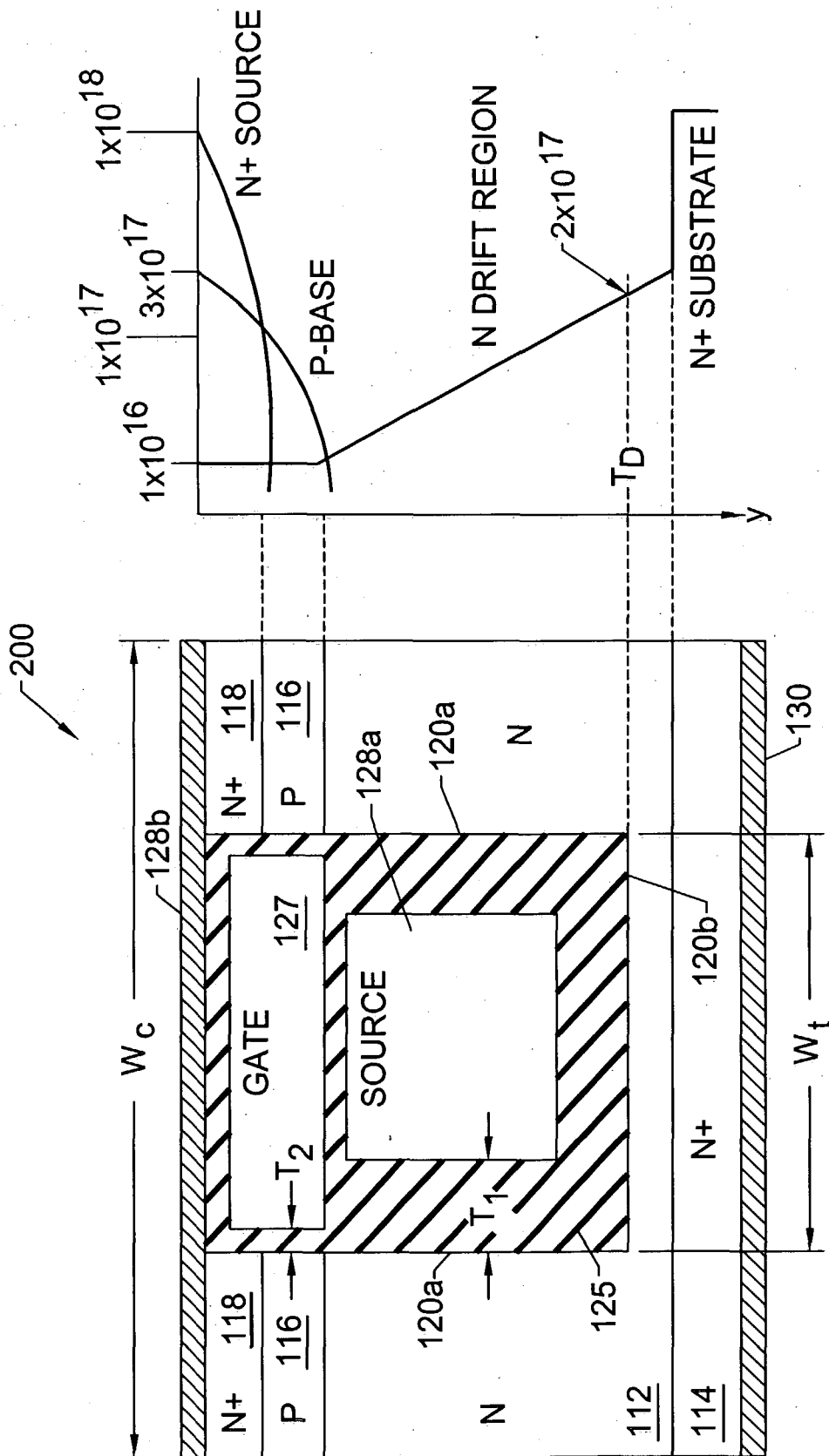


FIG. 3A.

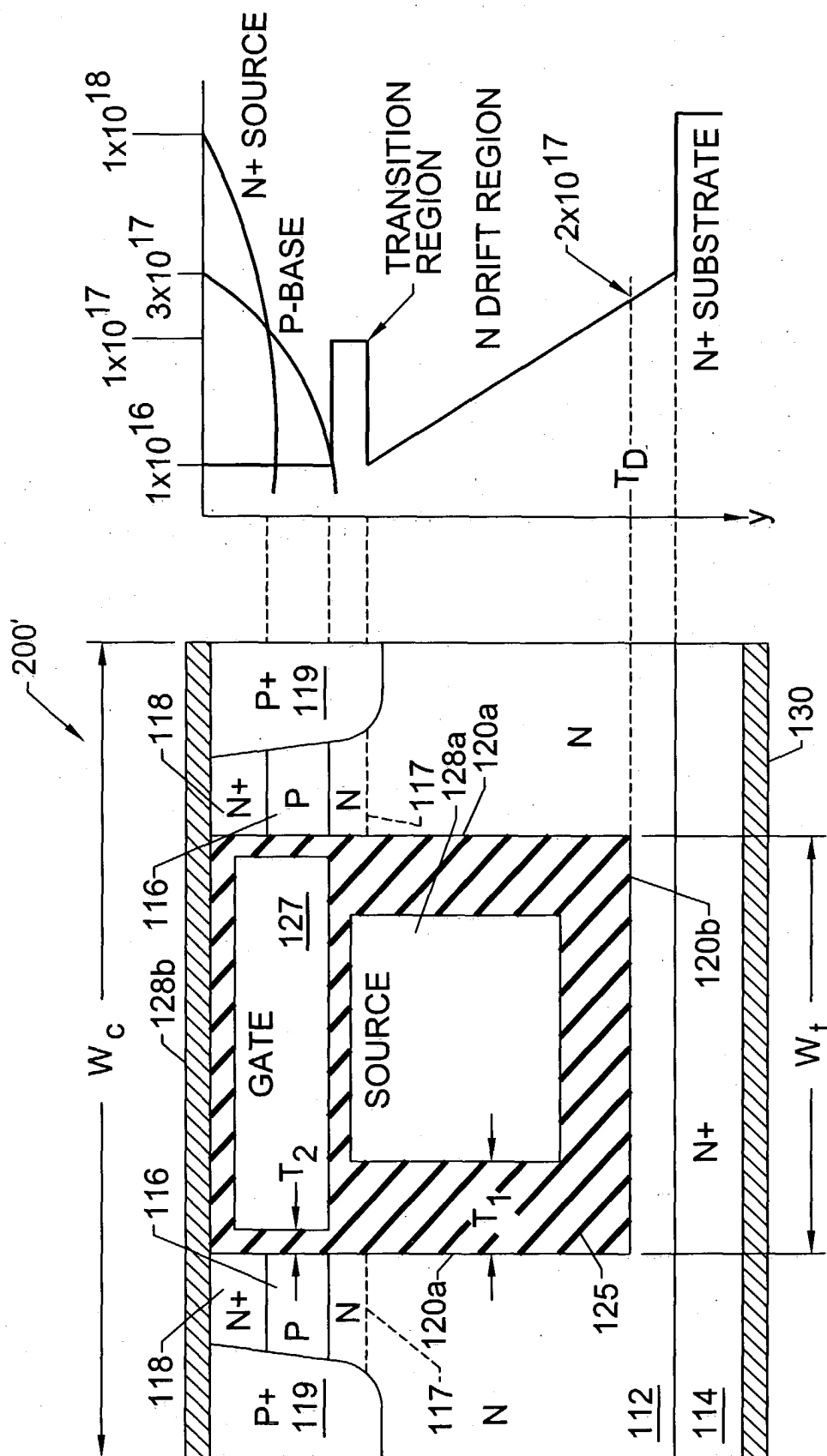


FIG. 3B.

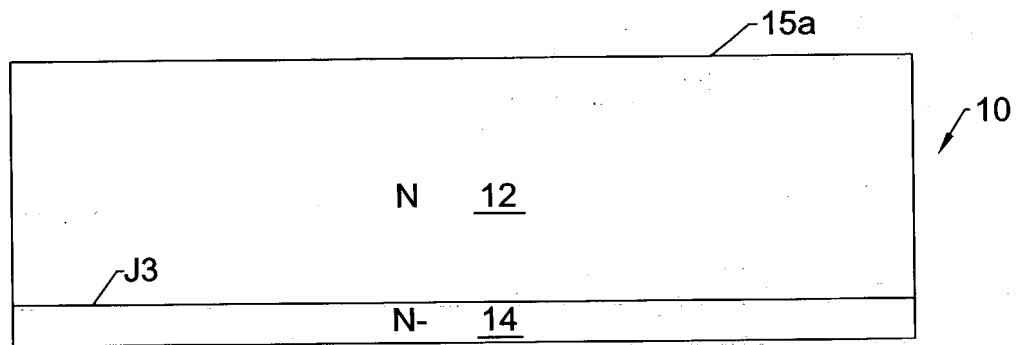


FIG. 4A.

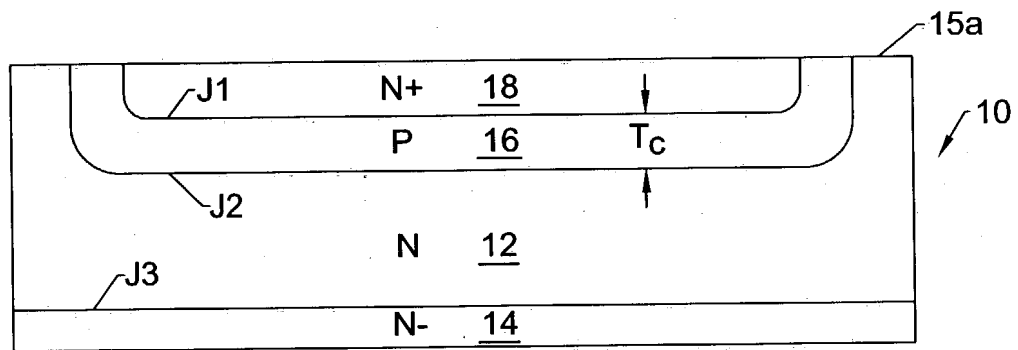


FIG. 4B.

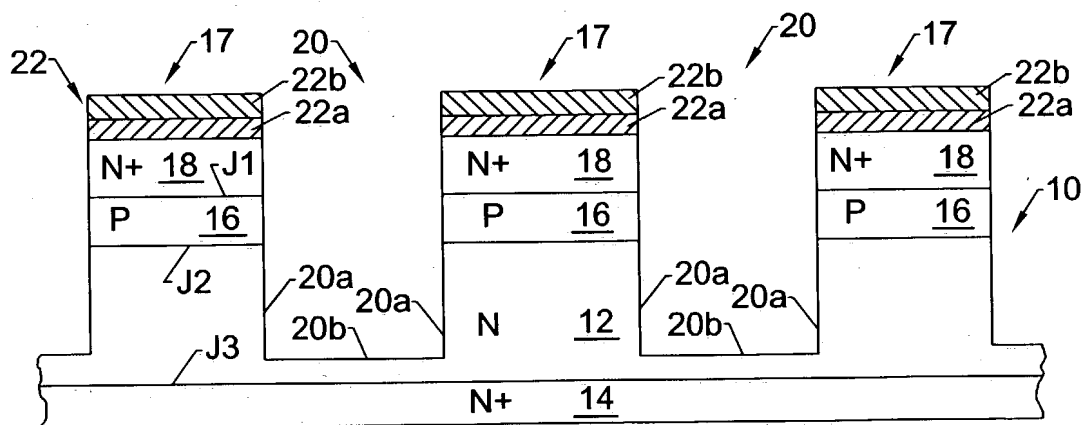


FIG. 4C.

This cross-sectional view shows three gate structures (22) on a substrate (10). Each gate structure consists of a gate stack (24) on top of a gate spacer (26). The gate stack (24) includes a top layer (22b) and a middle layer (22a). The gate spacer (26) is formed on the side walls of the gate stack. The substrate (10) is divided into regions (18, 16, 12, 14) by the gate structures. The regions (18, 16, 12, 14) are labeled with their respective dopant concentrations: N+, P, N, and N+. The regions (18, 16, 12, 14) are also labeled with their respective thicknesses: 18, 16, 12, and 14. The regions (18, 16, 12, 14) are also labeled with their respective material types: J1, J2, J3, and J4. The regions (18, 16, 12, 14) are also labeled with their respective electrical properties: 18, 16, 12, and 14. The regions (18, 16, 12, 14) are also labeled with their respective physical properties: 18, 16, 12, and 14.

[illegible]

FIG. 4F.

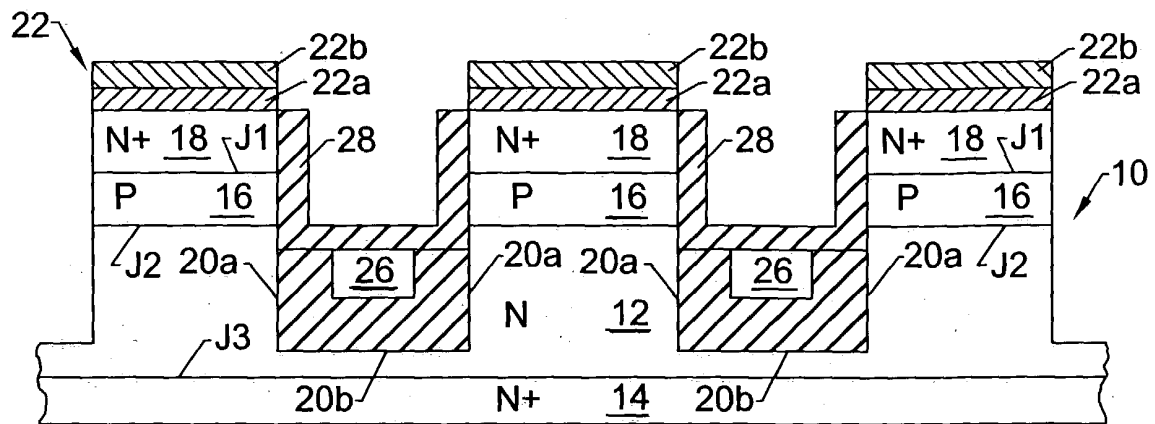


FIG. 4G.

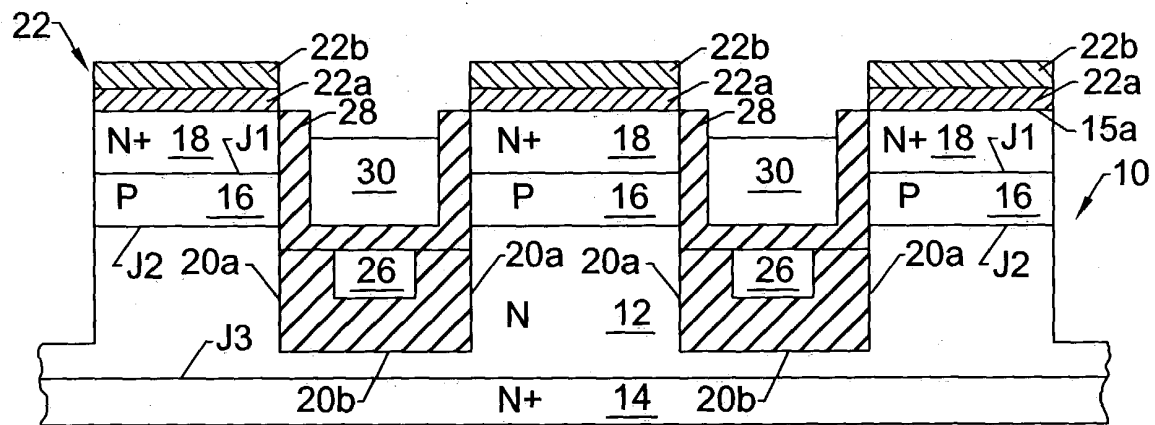


FIG. 4H.

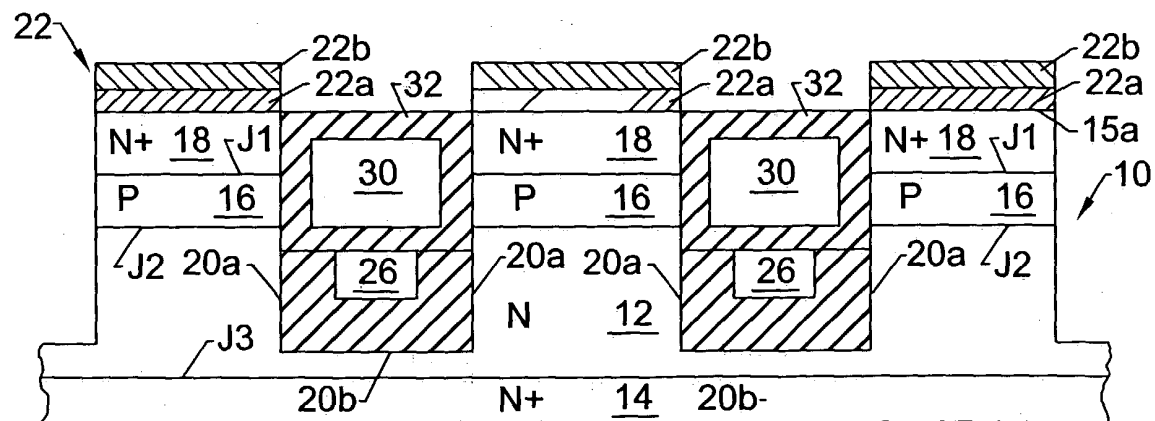
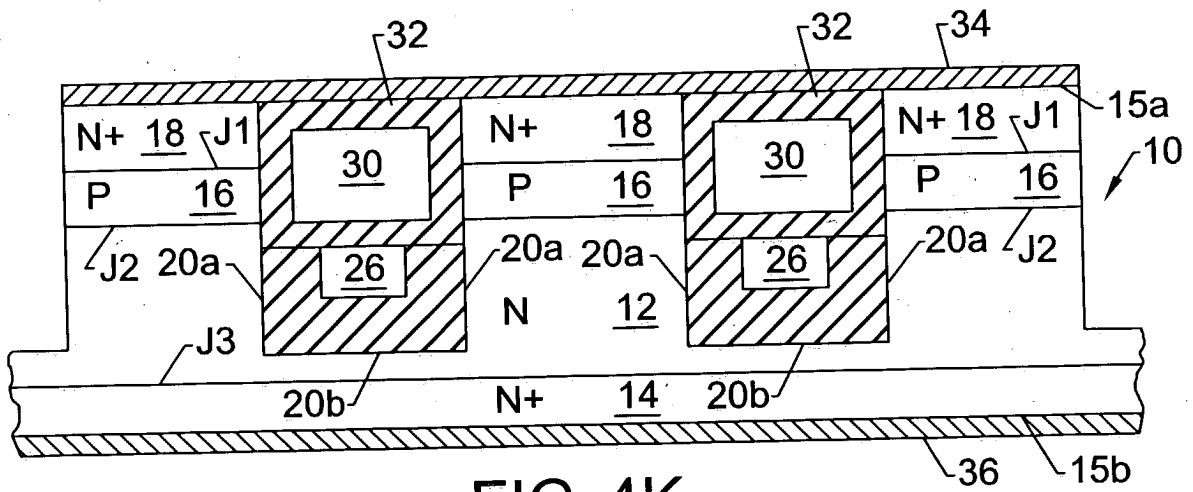
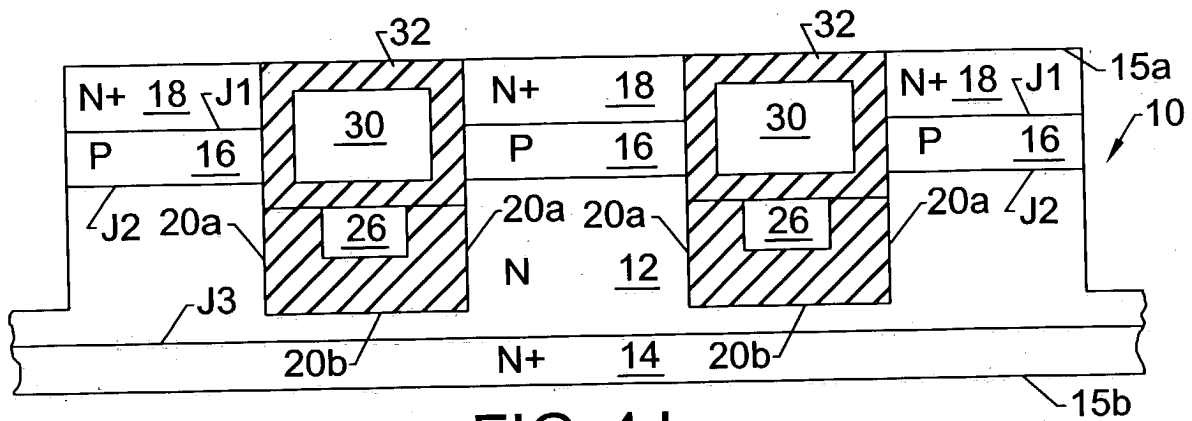
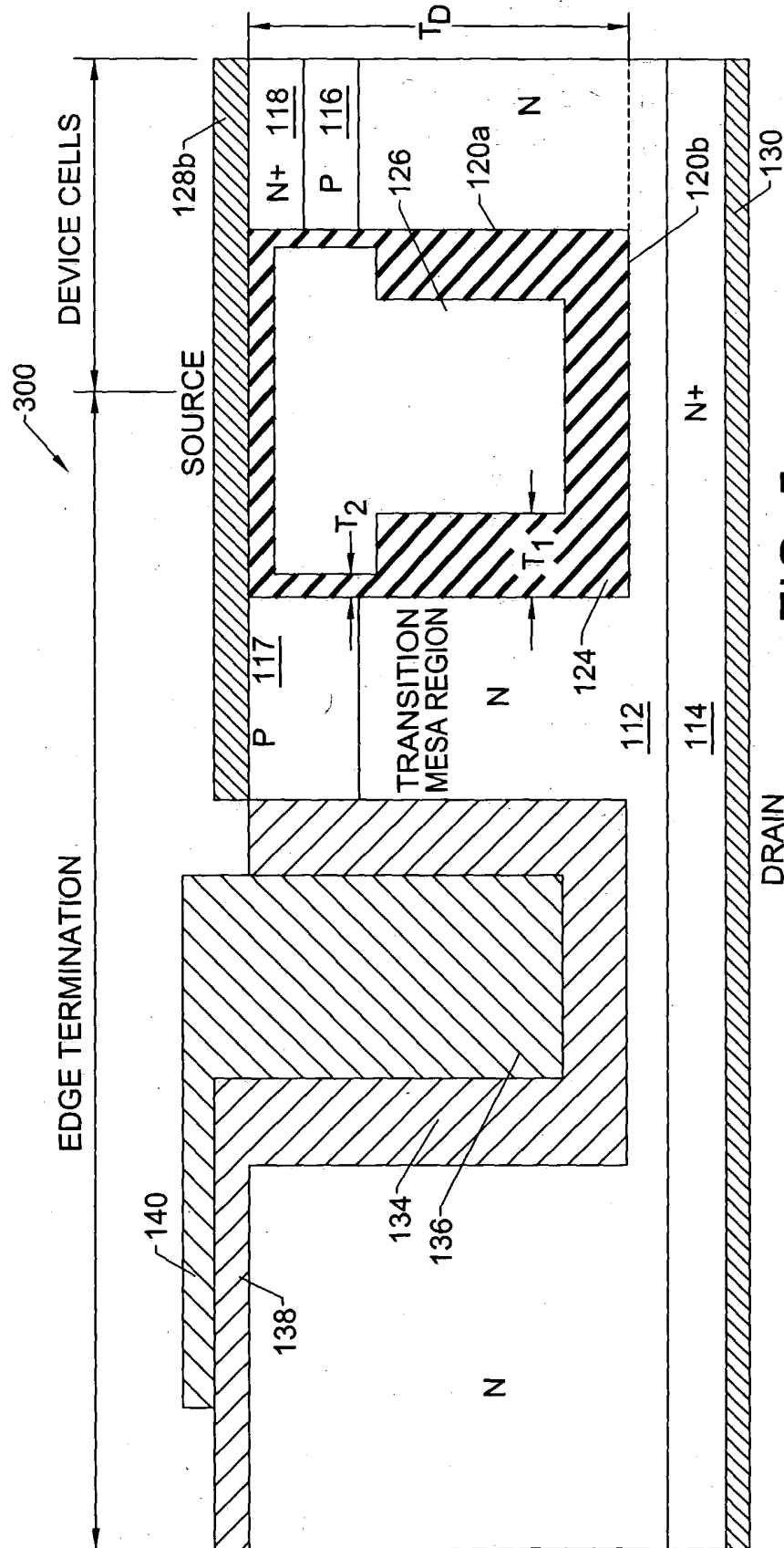


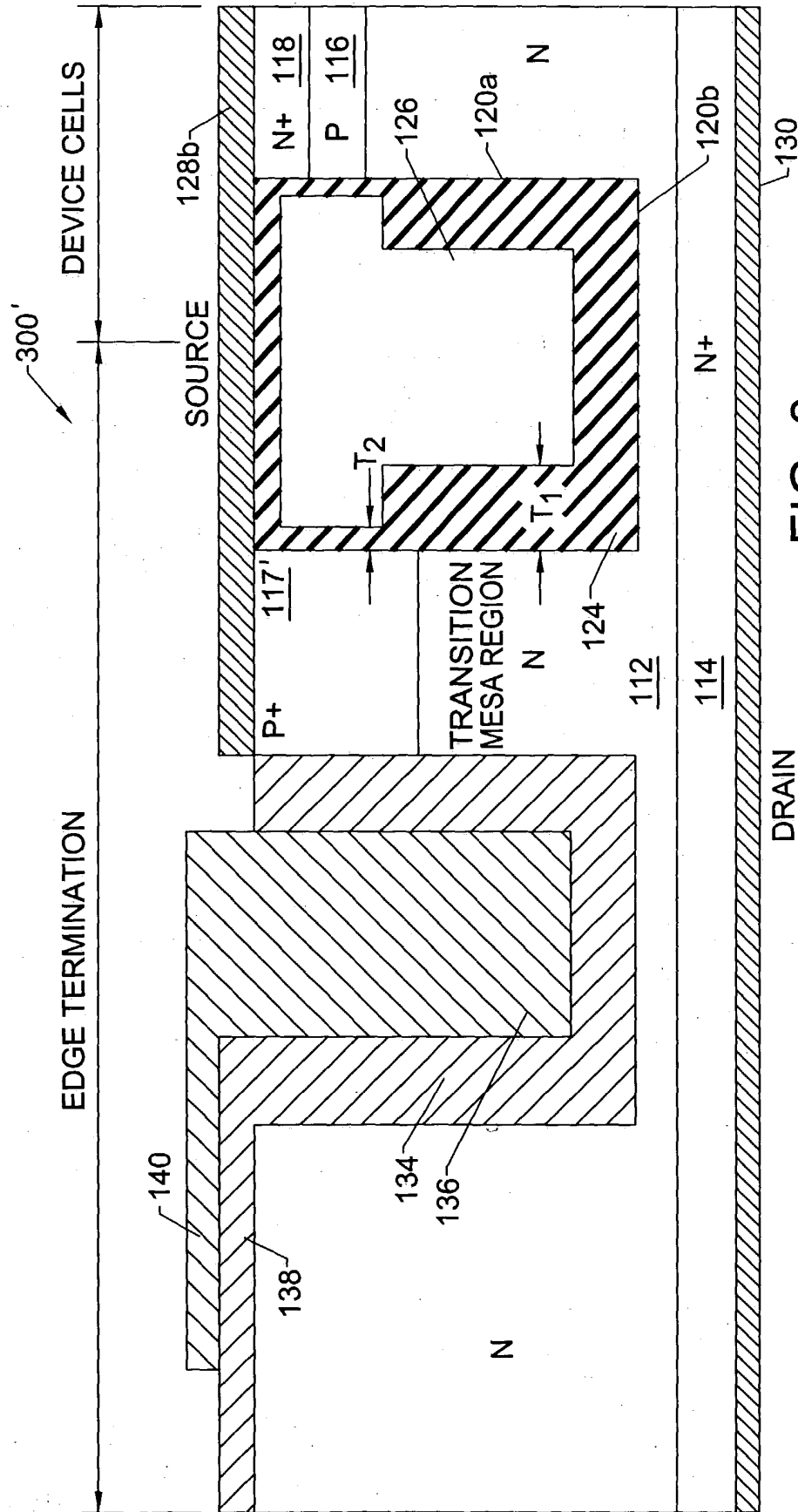
FIG. 4I.







**FIG. 5.**



**FIG. 6.**

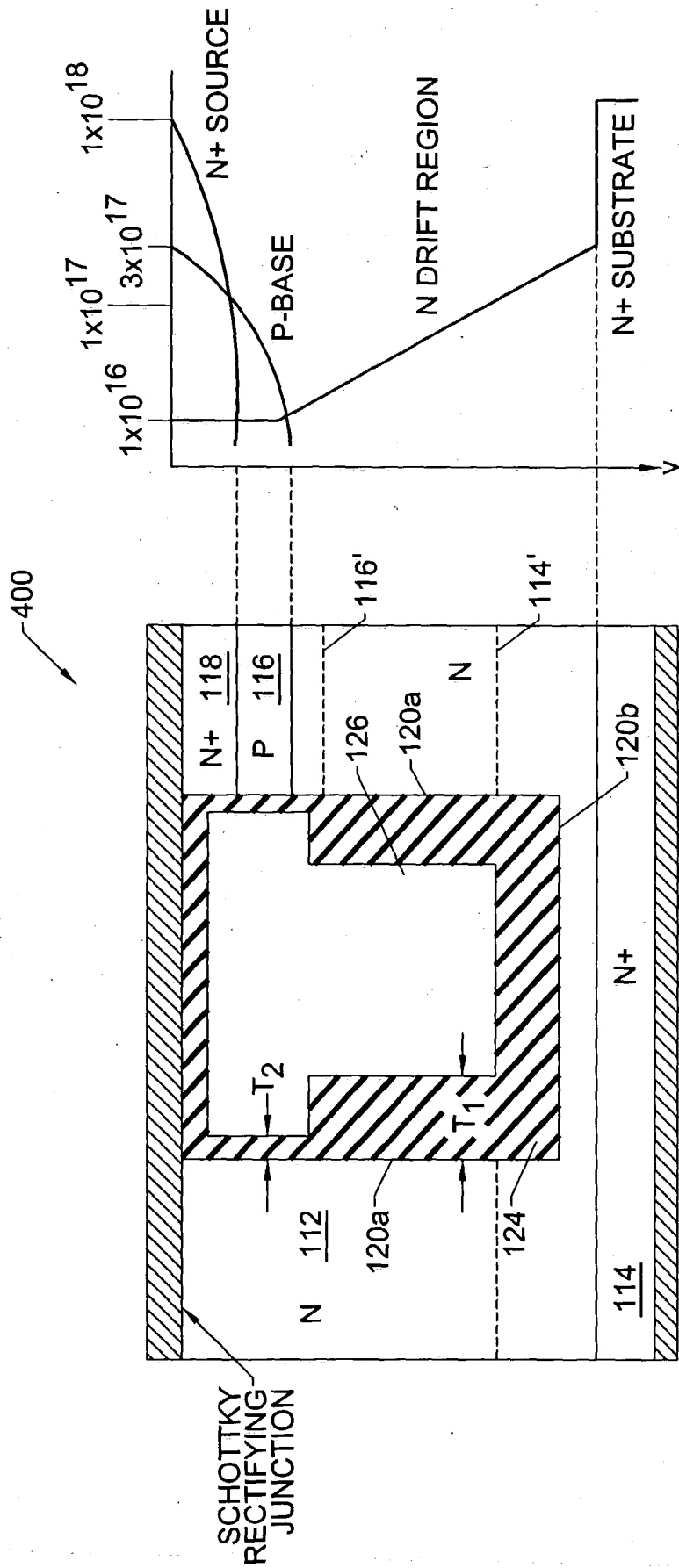
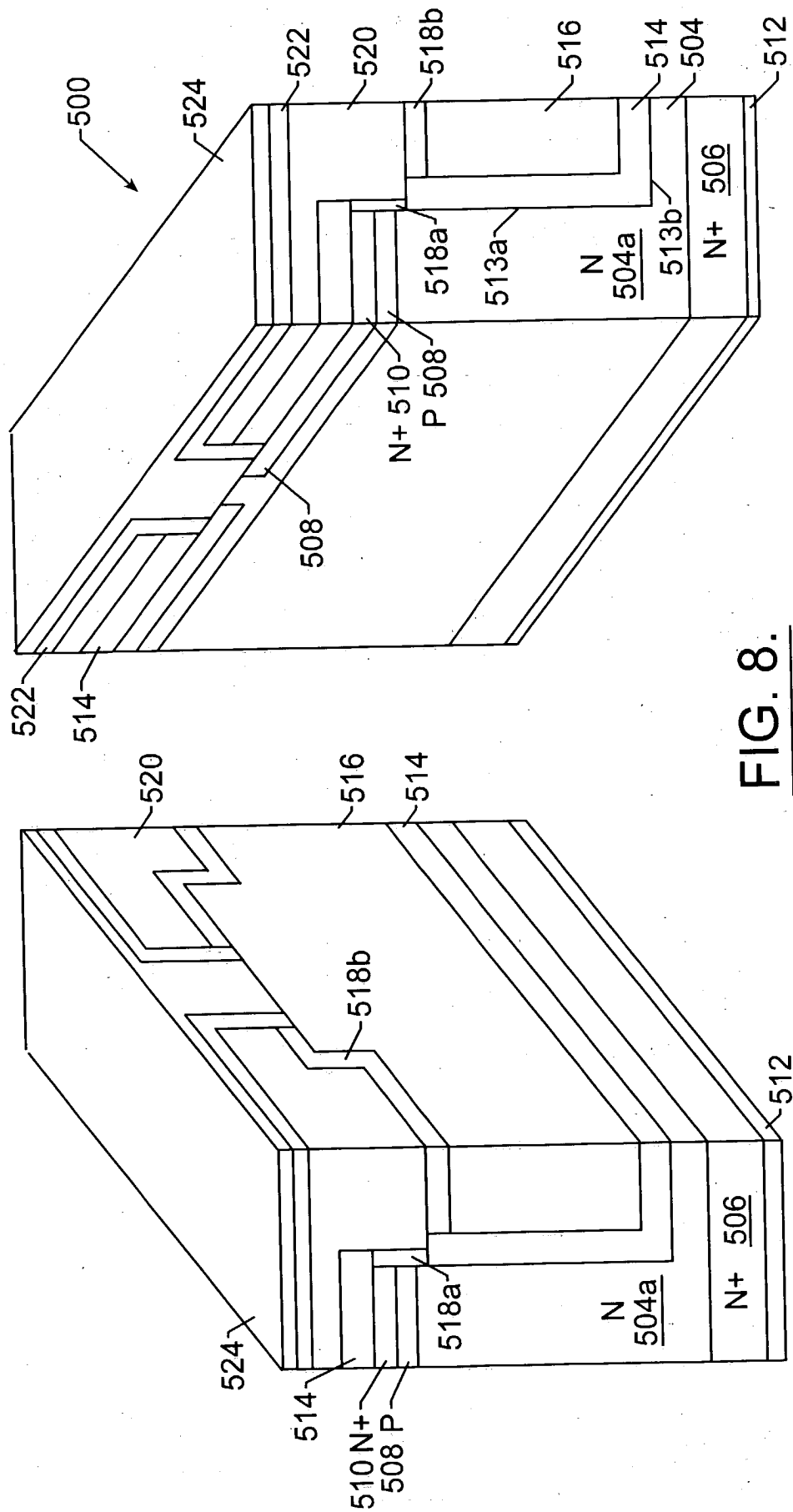


FIG. 7.



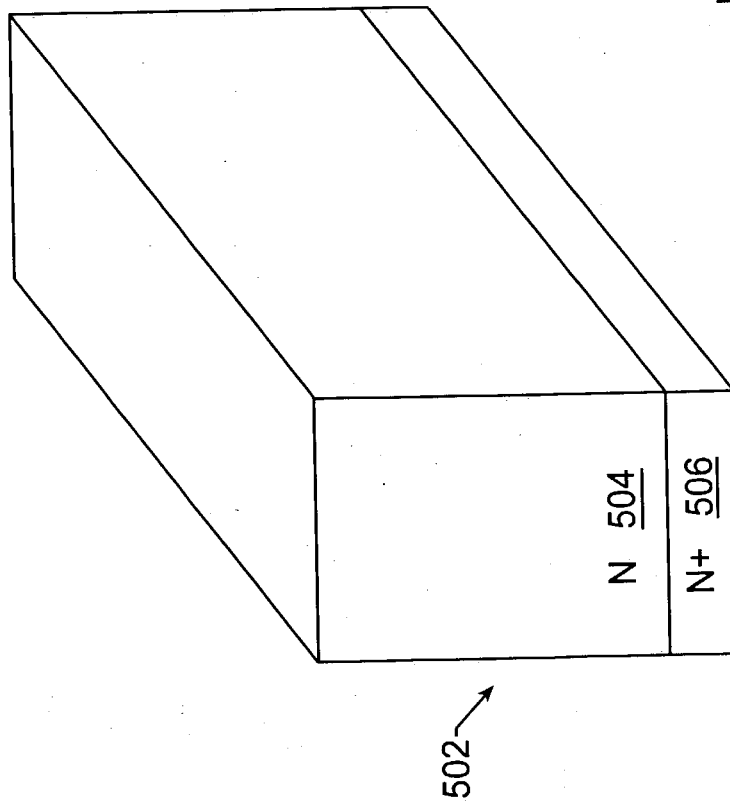
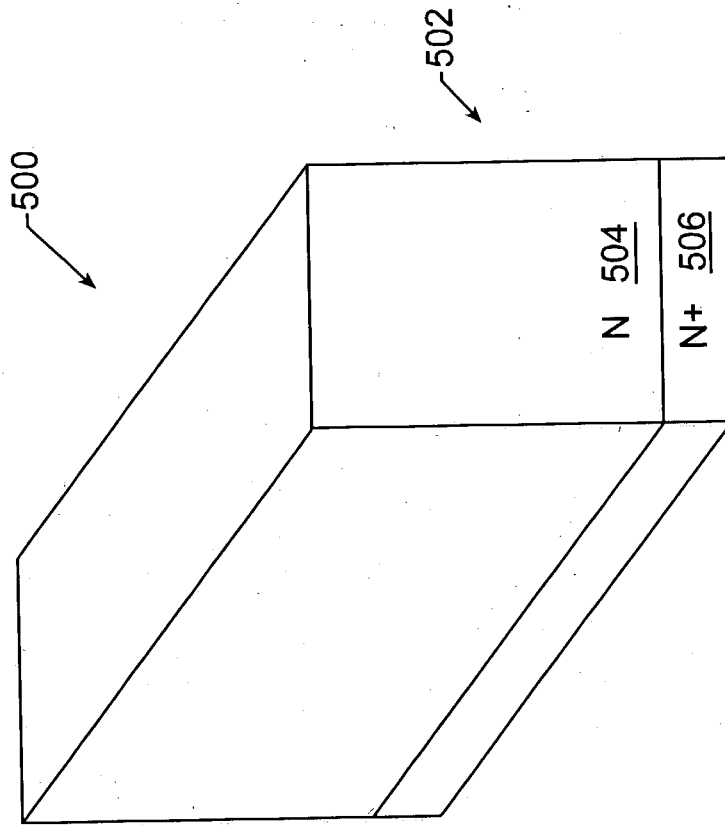
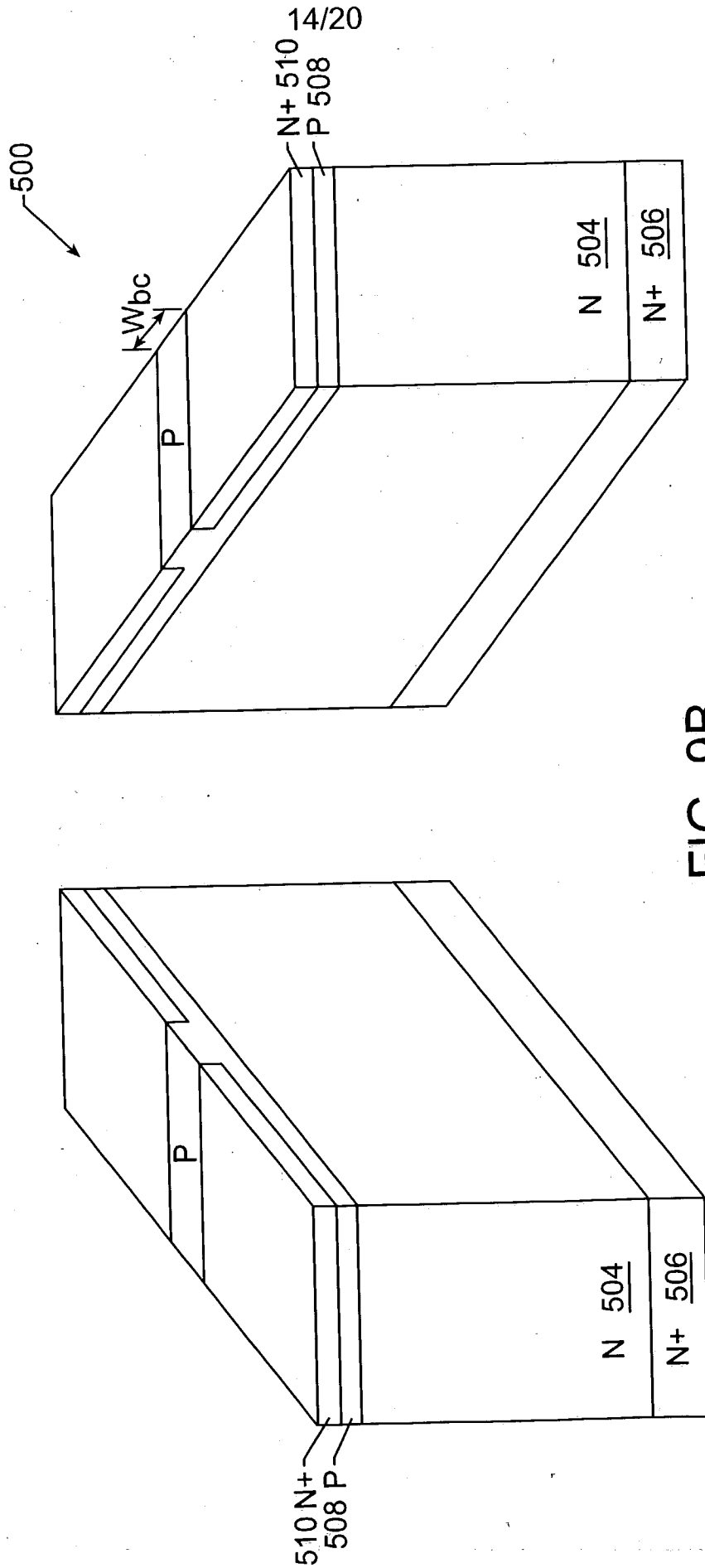


FIG. 9A.



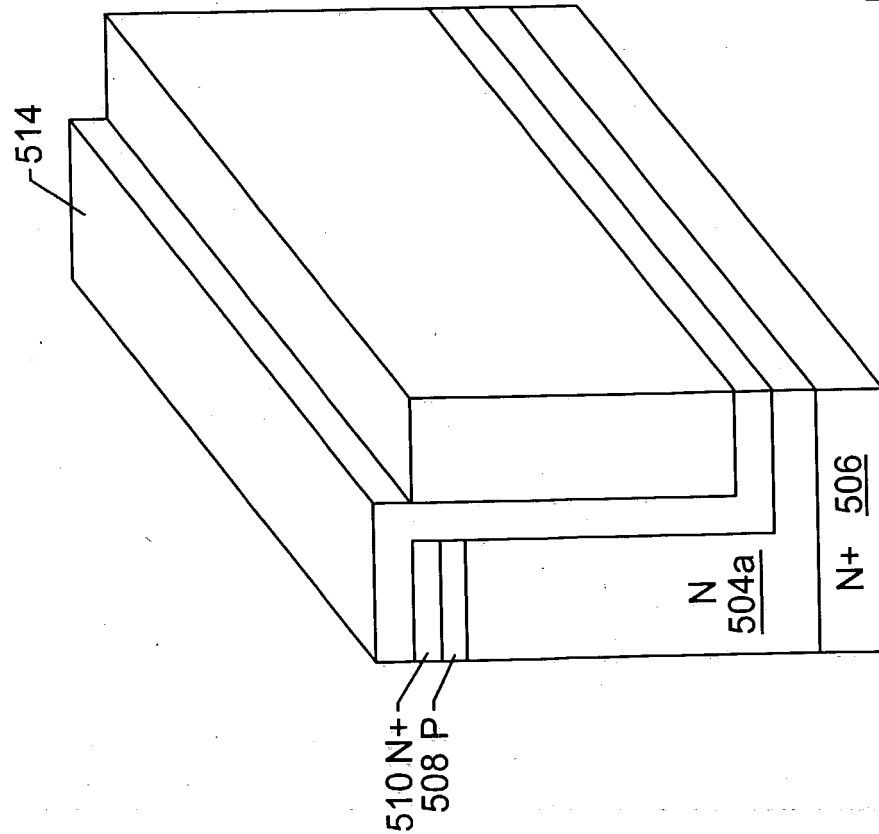
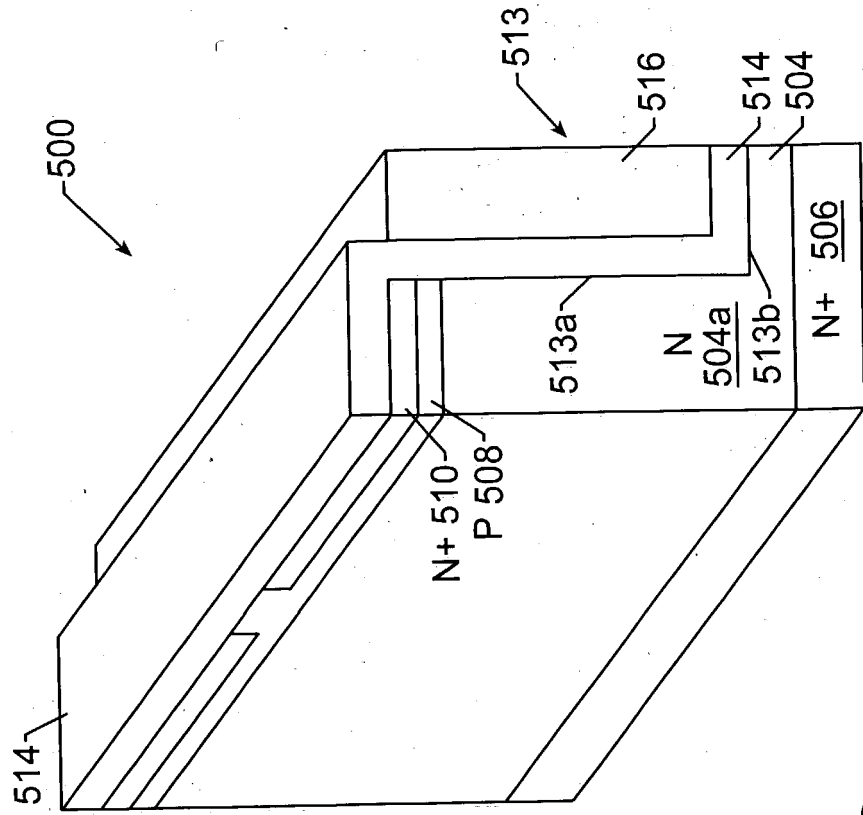


FIG. 9C.

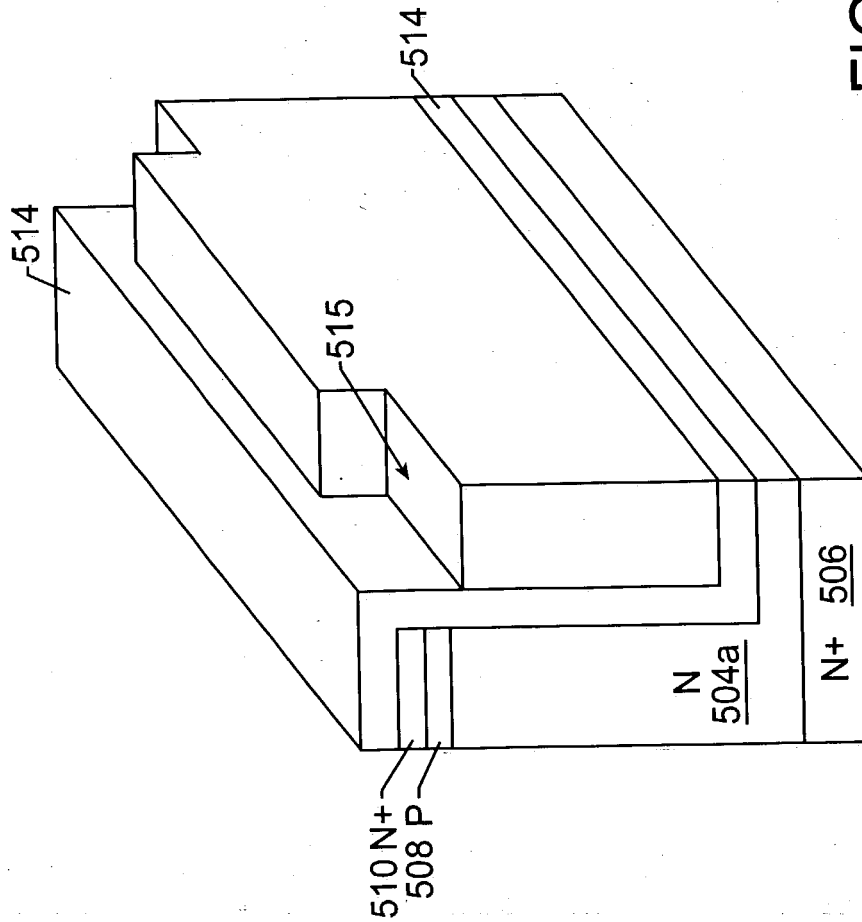
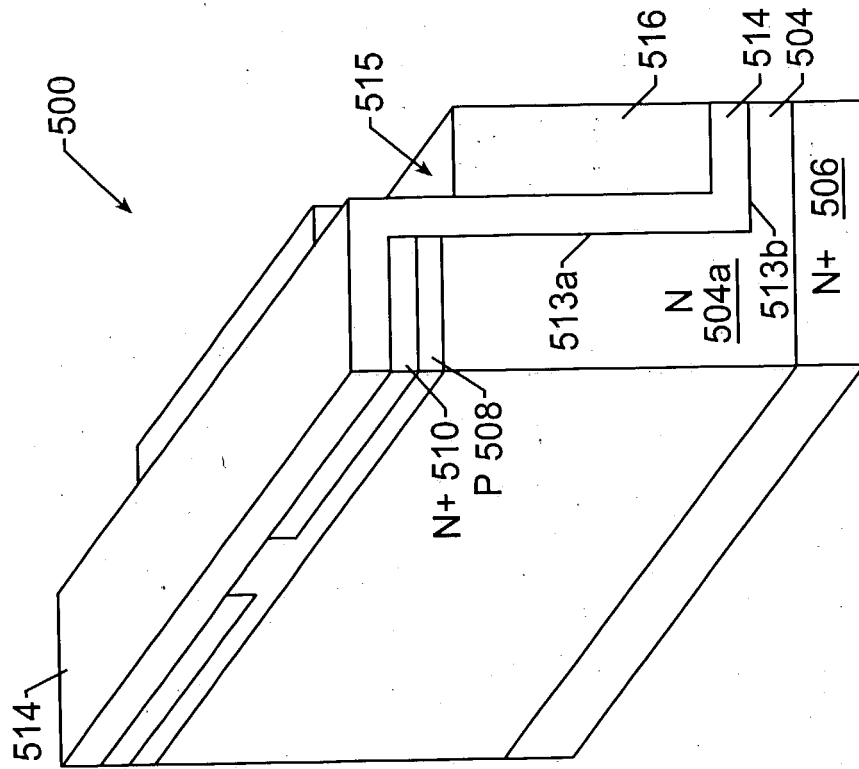


FIG. 9D.



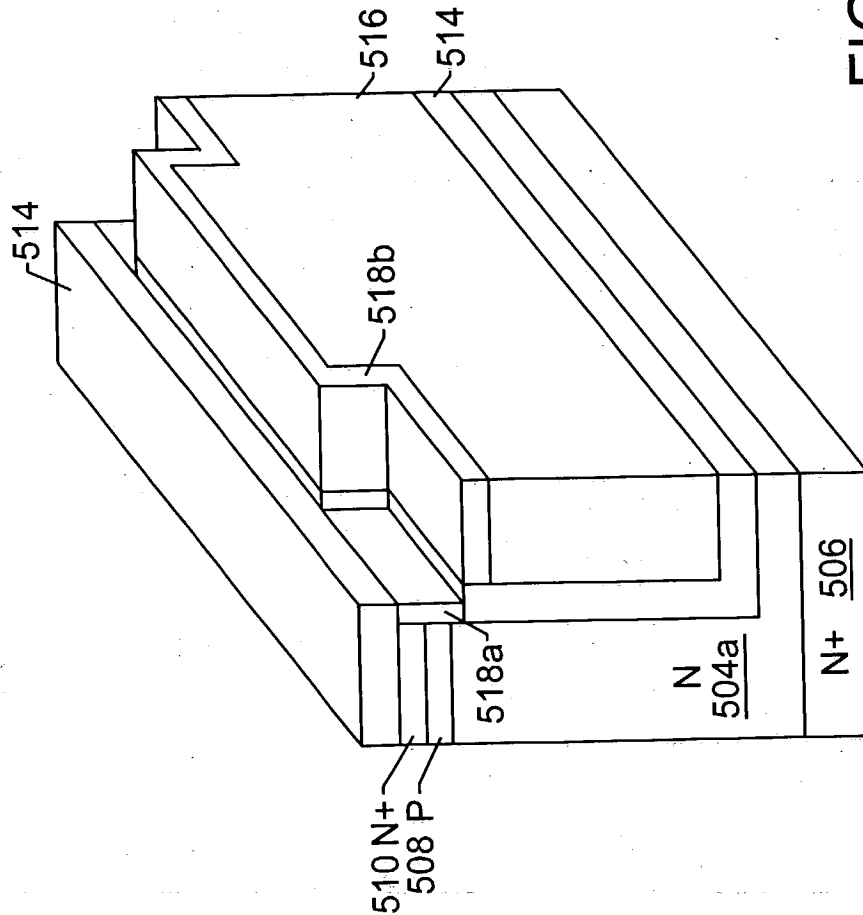
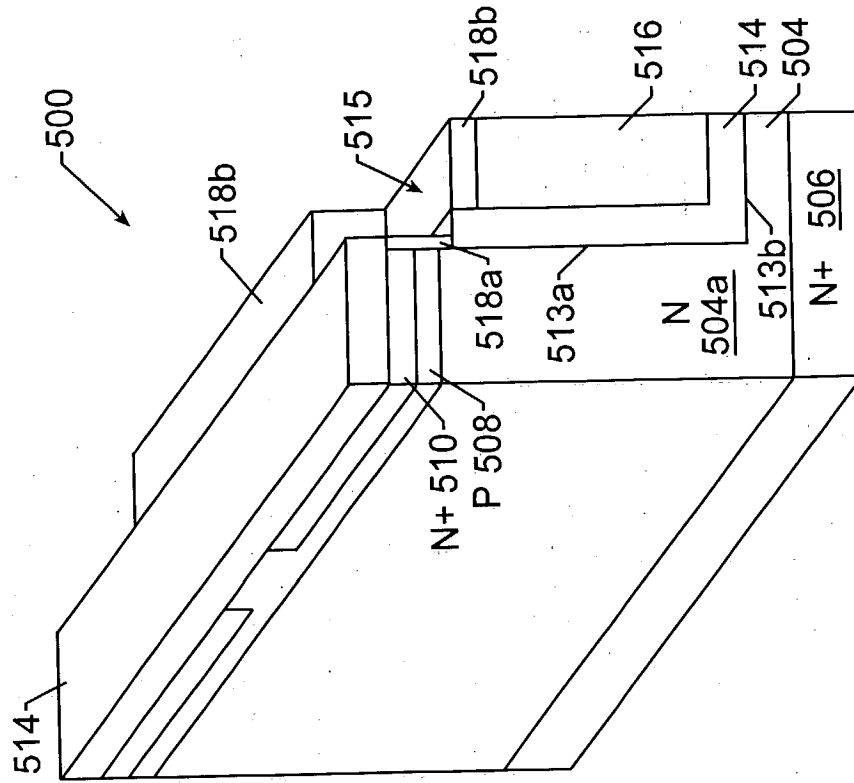


FIG. 9E.

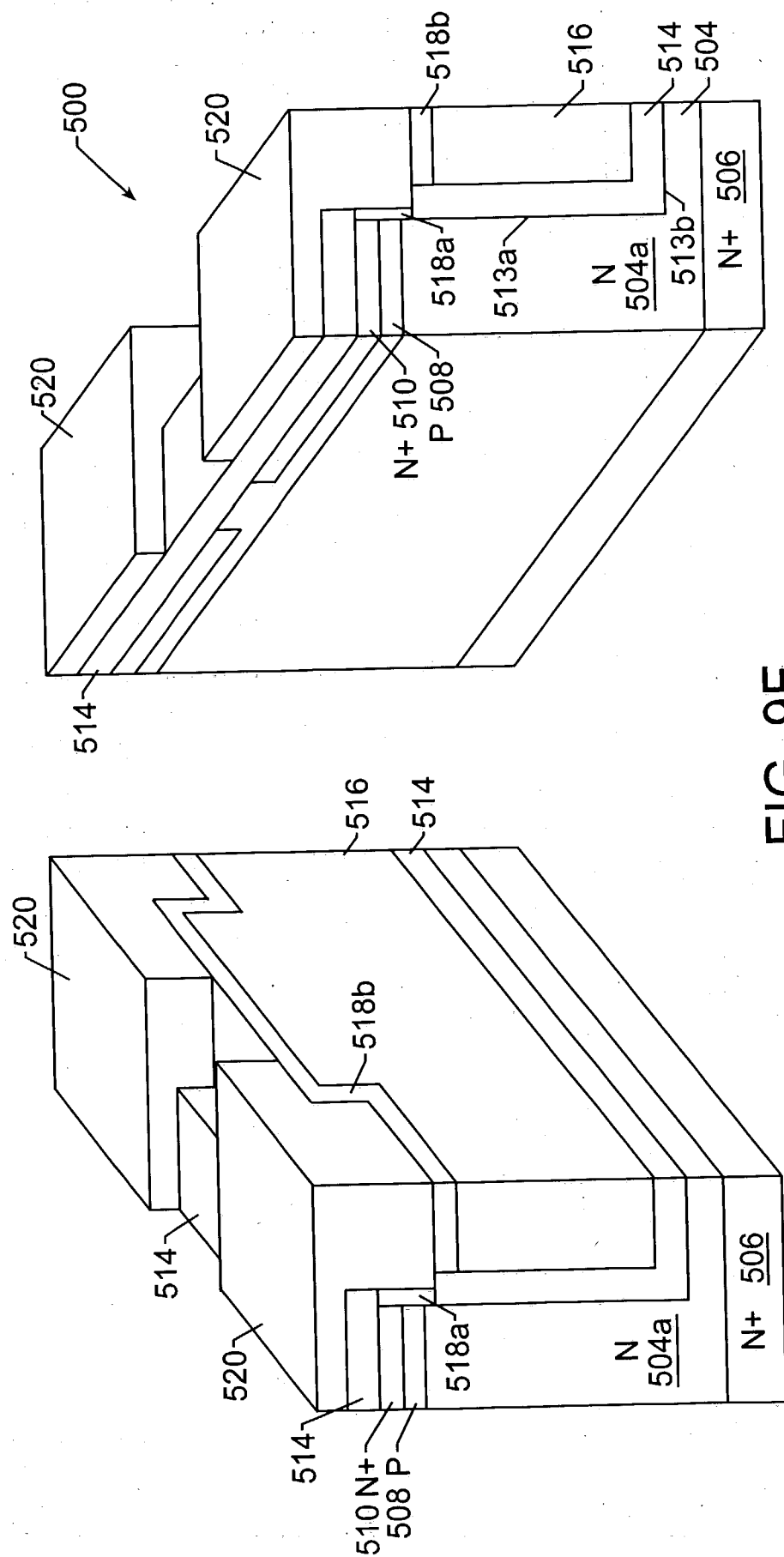


FIG. 9F.

